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**SIMULATION OF
DOUBLE BARRIER
RESONANT TUNNELING DIODES**

by

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SIMULATION OF

DOUBLE BARRIER RESONANT TUNNELING DIODES

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ABSTRACT

The double barrier resonant tunneling diode (DBRTD) is one of several devices currently being considered by the semiconductor inducstry as a replacement for conventional very large scale integrated (VLSI) circuit technology when the latter reaches its currently perceived scaling limits. The DBRTD was one of the first and remains one of the most promising devices to exhibit a room temperature negative differential resistance (NDR); this non-linear device characteristic has innovative circuit applications that will enable further downsizing. Due to the expense of fabricating such devices, however, it is necessary to extensively model them prior to fabrication and testing. Two techniques for modeling these devices are discussed, the Thomas-Fermi and Poisson-Schroedinger theories. The two techniques are then coompared using a model currently under development by Texas Instuments, Incorporated.

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I. INTRODUCTION

Microprocessor chips have doubled in speed approximately every 18 months since the mid 1980's. [Ref. 1] This increase in speed is due to improved circuit designs and smaller, more efficient very-large-scale-integrated (VLSI) circuit chips. The continued downsizing of these microprocessor chips certainly has a tangible limit; precisely when this limit will be realized is unknown at present. It is important, however, that the limit to continued miniaturization of VLSI technology will probably occur when device sizes have reached dimensions sufficiently small that quantum effects become significant. In Chapter II, several theoretical limits to continued downsizing of VLSI devices will be discussed. Among these is the need for an advanced lithography technique that can etch circuit designs onto chips and be commercially feasible. Assuming that advances in lithography are made, one alternative technology that utilizes the quantum mechanical properties of charge carriers is the evolving science of nanoelectronics. In Chapter III the basic building block of nanoelectronics, the double barrier resonant tunneling diode (DBRTD), will be discussed. Understanding the theory and operating characteristics of this device is important to assessing the potential impact of this new technology. Chapter IV will present two techniques for determining the flow (or confinement) of electrons in this basic device structure: the Thomas-Fermi and the Poisson-Schroedinger theories. The results of simulations using these two techniques will be compared. Specifically, the profiles of the electron potential energy and electron

densities throughout the device structure as well as the current-voltage characteristic will be shown for a typical GaAs / AlGaAs DBRTD.

II. LIMITS TO MICROPROCESSOR DOWNSIZING

A. THE TRANSISTOR AND PRESENT MICROPROCESSORS

The transistor is the basis for modern digital technology. It is effectively an electrical switch which when properly biased will either prevent or allow current to flow. Under the appropriate bias the saturation flow of current is typically considered a logical on or '1' state, whereas the lack of current is typically considered a logical off or '0' state. Combinations of these states ('1' and '0') are used to describe numbers and letters in binary, decimal, or hexadecimal representation. Groupings of these representations are then used via higher level languages (C, Pascal, Fortran, etc) to characterize the objects and occurrences in our world. Transistors grouped together and interconnected can be given a particular function. A 32 bit adder, for instance, typically requires on the order of 700 transistors. Figure 1 shows only one cell of 32 which are needed to construct a single parallel adder. Any number of other special purpose circuits can also be fabricated by properly interconnecting a sufficient number of transistors.

The modern microprocessor is effectively a very large number of transistors that are interconnected and placed on a silicon wafer. Fabricating all circuit elements on the same piece of silicon is referred to as an integrated circuit (IC). The science/art of integrated circuit technology is to maximize the operations performed by a given set of transistors. The improvement of microprocessors is, therefore, done in two basic ways: improve the circuit design to minimize interconnects and improve efficiency, or increase the number of

transistors for a given microprocessor. In the computer industry, both techniques are used simultaneously. For example, the Intel Pentium and Pentium Pro are

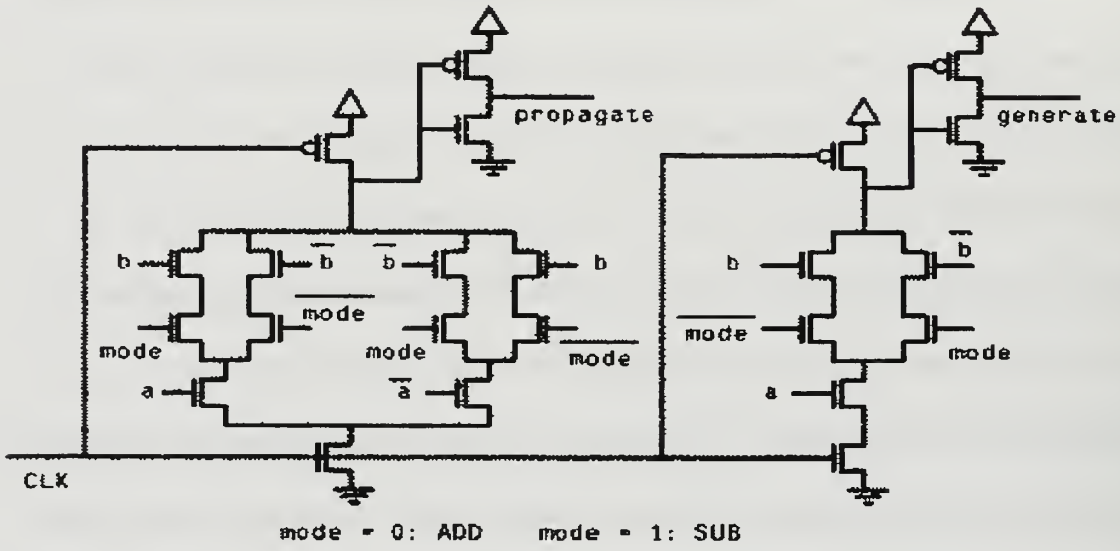

Figure 1 - A propagate/generate cell. 32 cells are needed to construct a single 32 bit adder. From Ref. [2]

fabricated with transistor element dimensions on the order of 0.35 micrometers (μ) as shown in Figure 2. This dimension is considerably smaller than previous generation processors whose transistor element dimensions were on the order of 0.65 μ. Pentium microprocessors also utilize superscalar concepts and parallel execution of instructions. Presently, the Pentium Pro chips have on the order of 5.5 million transistors arranged on a single chip. Future generations of chips are planned to scale down to transistor element dimensions of approximately 0.1 - 0.2 μ.

B. OBSTACLES TO FURTHER DOWNSIZING

As transistor dimensions have shrunk dramatically in the past 10 years, the question naturally arises of how small conventional transistors can be fabricated before the underlying physics will no longer support a continued reduction in size. At best, this is a very difficult question to answer and at the writing of this report the answer is not known. A first attempt at solving this problem is to simply employ the knowledge base currently used to develop VLSI

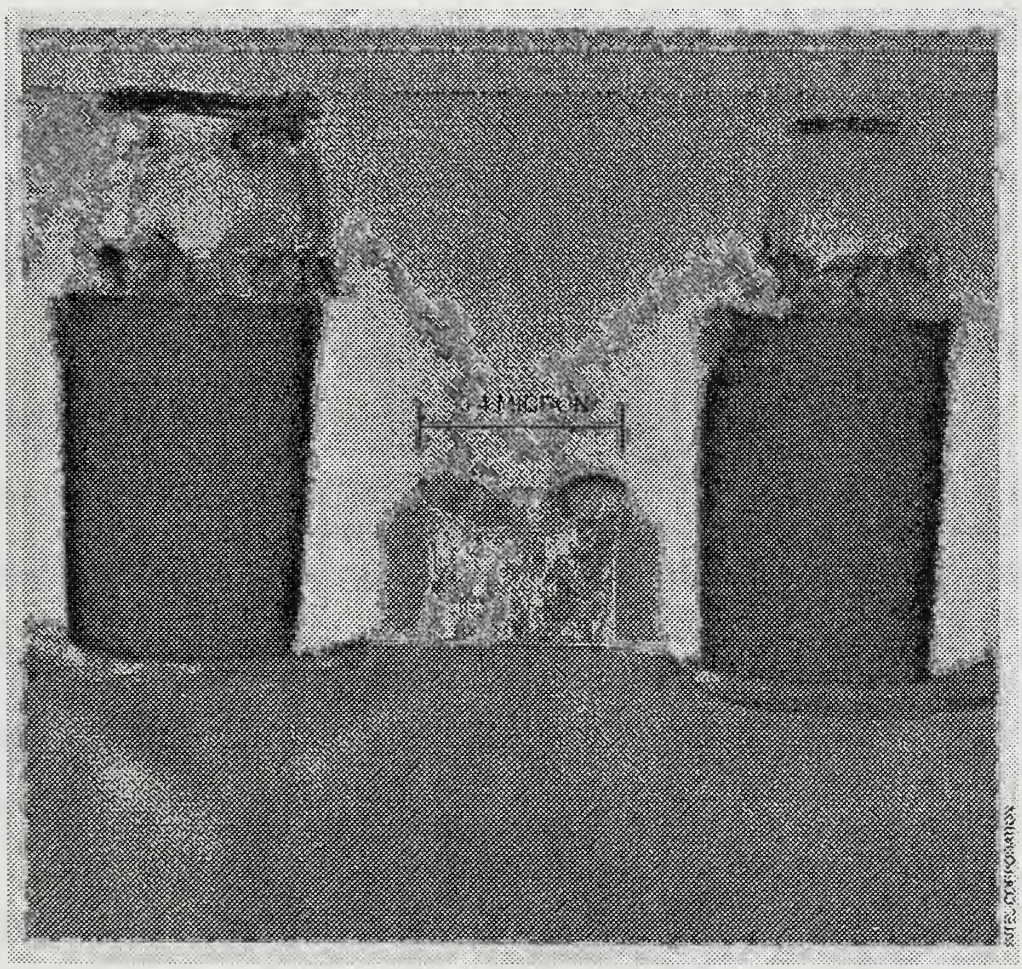

Figure 2 - State of the Art transistor with element dimensions of 0.35 μ
From Ref. [1].

circuits and simply scale the circuits to smaller dimensions.This approach unfortunately is not reliable simply because much of our understanding of device technology is experimentally derived and empirical in nature. It is difficult to generalize such empirically derived knowledge as succeeding device generations are made progressively smaller. In particular, these empirical relations do not apply to device dimensions much below 0.3 microns. [Ref. 3] It is, however, interesting to discuss a few of the limitations which are known but not completely understood or quantified.

One limitation to the downsizing of transistors in VLSI circuits is the need for input-output isolation. Figure 3 is a diagram of a basic enhancement

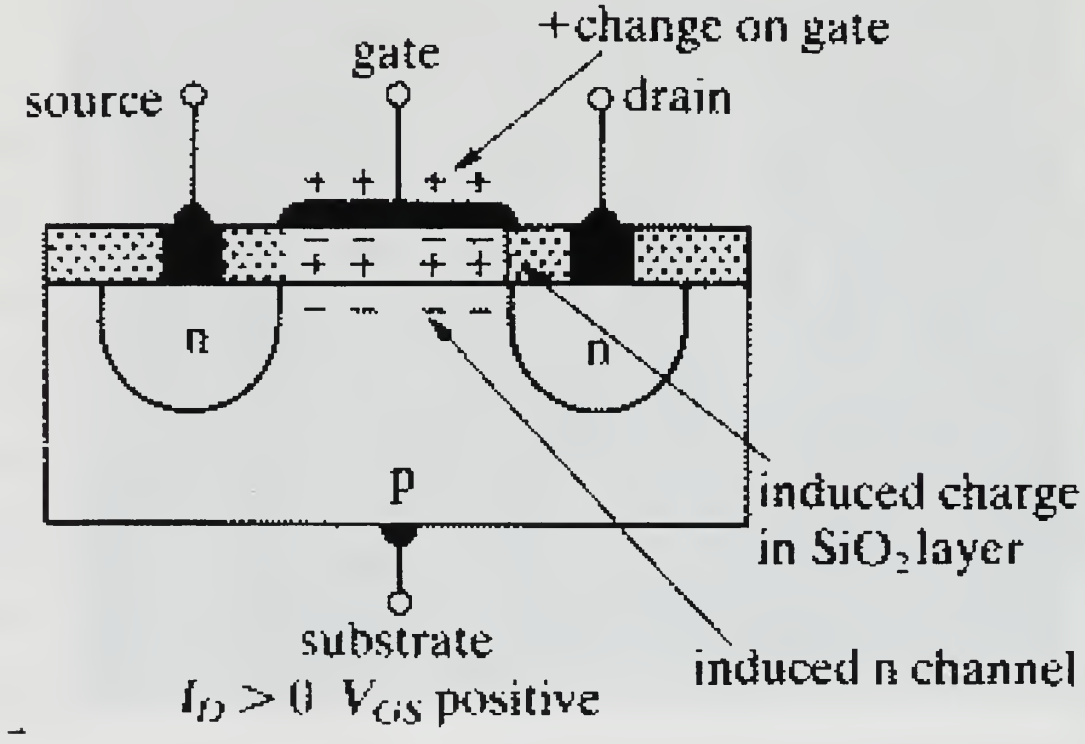

Figure 3 - Enhancement n-channel MOSFET. From Ref. [4]

n-channel metal oxide semiconductor field effect transistor (MOSFET). With no bias applied to the gate, the device is off. When a positive bias is applied to the gate (with respect to the source), the device is on and current flows. The gate bias induces a positive charge in the silicon oxide layer which in turn induces a negative charge near the oxide/p-type boundary. This induced negative charge creates a channel through which current can flow. In order for the effect to occur, however, the silicon oxide layer must be thick enough to electrically isolate the gate from the p-type layer. This thickness is known to be limited to 30 angstroms or greater before tunneling will occur between the gate and p-type substrate. If such tunneling were to occur, it would form a leakage path through the device, effectively preventing the device from being in an off state.

Another isolation related phenomenon is gate-induced drain leakage. As the overall dimensions of the transistor are reduced, the width of the silicon dioxide layer, which isolates the gate from the drain, is also reduced. As this width is reduced, the effect is a gradual reduction in the threshold gate voltage. In the case of the n-channel enhancement MOSFET, the device will eventually not be capable of turning off. Conversely, in the case of the n-channel depletion MOSFET, the device will not be capable of turning on.

Still another effect of down-scaling transistors is a reduction in the junction depths. In other words there is simply less material between the source and substrate or the drain and substrate. One effect of reduced junction depth is a lower breakdown voltage between source/substrate and drain/substrate. Another effect is that the series resistance of these transistors is increased due to the

smaller surface areas of the contacts. Finally, with shallower junction depths, the probability of leakage due to fabrication flaws is dramatically increased.

Only a few of the effects of down-scaling transistors have been discussed here. In a comprehensive study several other effects must also be studied. Such effects, though very important, will not matter unless an advanced lithography technique for manufacturing scaled-down devices is discovered. VLSI circuit chips are currently mass produced using photolithography.

> In photolithography, light is used to transfer circuit patterns from a quartz template, or mask, onto the surface of a silicon chip. The technique now fashions chip features that are some 0.35 micron wide. Making features half as wide would yield transistors four times smaller, since the device is essentially two-dimensional. [Ref. 5]

Making devices substantially smaller will become increasingly difficult as the diffraction limit of conventional lithographic light sources is approached. Many companies have invested in x-ray lithography as an alternative. At present, however, it does not appear that x-ray lithography can be commercially feasible. Another technique is known as electron beam lithography. Currently, however, electron beam lithography must be done serially, one "line" at a time, similar to writing the circuit diagram onto a chip. This process is slow and not practical for mass production of VLSI chips, for which a parallel writing technology would have to be developed.

C. NANOELECTRONICS

The limits to downsizing of VLSI technology may not be reached for several years to come, but eventually they will be reached. There are alternative technologies currently under research to replace conventional transistors. One

such technology has been termed nano-electronics, indicating the scale of device structure that is envisioned. As alternative fabrication techniques are explored it is prudent to develop a working knowledge of the device physics through a joint effort of modeling and fabrication. In this way, when practical mass fabrication processes do become available, there will already be in place an understanding of the individual devices and circuit designs. Such circuit designs will have to include a method for interconnecting individual elements.

Currently, all approaches for developing a practical, room-temperature nanoelectronic technology are based on the device structure depicted in Figure 4 which is commonly called the double barrier resonant tunneling diode. The DBRTD has transfer characteristics which make it desirable for use in high speed switching applications (on the order of 10^{12} Hz). [Ref. 6] Of greater importance from a research standpoint is that it is the building block for developing a resonant tunneling transistor, in analogy with the conventional diode structure (a simple p-n junction device) which is the building block for various types of conventional transistors. The DBRTD is referred to as a heterostructure device. Semiconductor heterostructures are formed from dissimilar semiconductors with differing band gaps. At the bottom of Fig. 4 is shown the conduction band profile that arises as an electron moves vertically through the sequence of semiconductor layers shown in the top half of the figure. In the next chapter some of the basic physical principles underlying the operation of resonant tunneling diodes will be discussed.

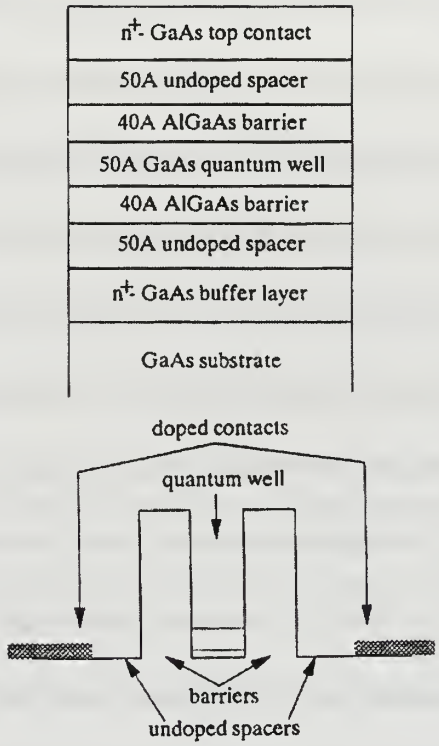

Figure 4 - Structure and conduction band profile of a typical GaAs / AlGaAs DBRTD. From Ref. [6].

III. THE DOUBLE BARRIER RESONANT TUNNELING DIODE

A. ELECTRON TRANSPORT IN SEMICONDUCTORS

The electron is classically considered a particle but quantum mechanically described as a particle and a wave. Electrons, therefore, can exhibit wavelike characteristics such as diffraction and interference. The deBroglie wavelength of a free electron at room temperature (300 K) with an energy of 0.025 eV can be determined using Eq. 1 to be approximately 10 nm. In semiconductors this

$$\lambda = \frac{h}{\sqrt{2mE}} \qquad (1)$$

wavelength is even larger because of the electron's relatively small effective mass. In GaAs, for example, $\lambda \sim 30$ nm at room temperature. The electron wavelength sets a rough distance scale at which a quantum description of a device becomes necessary. At these size scales, quantum mechanics must be used to understand how electrons will behave. Using quantum mechanics, a wave function (Ψ) is associated with a particle with the interpretation that the square of the wave function is the probability density of finding the particle at a location (z). $\Psi(z)$ is obtained from the solution to Eq. 2 (Schroedinger's Eq.).

$$\frac{-\hbar^2}{2m}\nabla^2\Psi + U\Psi = i\hbar\frac{\partial\Psi}{\partial t} \qquad (2)$$

$\hbar$ = Planck's Constant (6.626×10^{-34} J - s) / 2π

m = electron mass (9.1×10^{-31} kg)

U = potential energy function

To understand the transport of electrons in semiconductors it is necessary to first understand their allowed energy bands which are determined from the time-independent Schroedinger equation with a periodic potential energy function appropriate to crystalline solids. Basically, if several atoms of a semiconductor are brought together to form a crystal, the discrete energy levels of the atoms broaden to form energy bands in the crystal. Each of the quantum states of the free atoms gives rise to one energy band in the solid. "The bonding combinations of states that were occupied by the valence electrons in the atom become the valence bands of the crystal. The anti-bonding combination of these states become the conduction bands". [Ref. 6] The form of the wave function in the periodic potential energy environment of a crystal is specified by the Bloch theorem (Eq. 3). [Ref. 7]

$$\Psi_{n,k}(r) = u_k(r)e^{-ik\bullet r} \qquad (3)$$

n = energy band index

k = wave vector

$u_k(r) = u_k(r+a)$ = periodic function of the crystal lattice

a = lattice constant of the solid

These wave functions (Ψ_κ) are found from the solution to the Schroedinger equation. If the energy levels associated with the energy bands (n) are plotted with respect to the wave vector (k), the resulting graph represents the energy band structure, $E_n(k)$.

Energy band theory only applies for perfectly periodic crystals and strictly only under zero bias. A practical semiconductor device will, of course, be subject to different bias states and will consist of compound materials, breaking perfect periodicity. Instead of seeking rigorous solutions to the Schroedinger equation for these situations, a more useful but approximate theory is used that accounts for the potential due to a periodic lattice (as band structure does), the potential due to an applied bias and the effects of compound materials.

The "effective mass" theory approximates the wave function as the product of an atomic part and a more slowly varying envelope function, with the electron mass in the Schroedinger equation replaced by the effective mass (m^*), a material dependent parameter. The resulting form of the effective-mass Schroedinger equation is given in Eq. 4. [Ref. 6]

$$-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2}\Psi + [E_n - qV(z)]\Psi = i\hbar\frac{d\Psi}{dt} \qquad (4)$$

$\hbar$ = Planck's constant (6.626×10^{-34} J - s) / 2π

m^* = effective mass (GaAs $m^* = 0.067 \times m_e$)

E_n = energy at edge of the n^{th} band

q = 1.6×10^{-19} coulombs

V = electrostatic potential function

Ψ = wave function or envelope function

The effective mass theory is an approximation and may not be valid under a large applied bias or for very a small length scale, e.g., at the level of a few atoms. The effective mass theory, however, enables us to analyze a variety of

compound-semiconductor device structures. In essence this theory replaces the full energy band structure of the electron, which arises from the rigorous solution of the Schroedinger equation, with a parameter, m^*, describing the effective inertia of the electron in a given energy band. Effective mass theory treats the electron in an energy band as if it were a fictitious free particle with an altered mass, m^*. Thus, effective mass theory assumes the energy-wavevector relation is given by $E(k) \approx \frac{\hbar^2}{2m^*}k^2$. [Ref. 6] This approximation can, therefore, be expected to be most accurate at the extremum of an energy band; for example, at the bottom of the conduction band for electrons. Having made the effective-mass approximation, we can readily analyze heterojunction devices using the familiar methods of elementary quantum mechanics.

B. RESONANT TUNNELING IN DOUBLE BARRIER HETEROJUNCTIONS

Quantum mechanical tunneling is a process whereby a particle passes (or "tunnels") from one classically allowed region to another through a classically forbidden region. Resonant tunneling is an enhanced tunneling process that can occur when the wavelength of the electron is approximately matched to the dimensions of the tunnel barriers. To understand nanoelectronics, it is necessary to first understand how an electron can tunnel through the double barrier structure (see, for example Fig. 4) since "resonant tunneling provides the basis for nanoelectronic logic and memory applications". [Ref. 8]

A key feature of heterostructures is that the semiconductor materials have different band gaps. For an electron in the conduction band, say, these

differences in band gaps present large variations in potential energy as electrons pass through the layers of a heterostructure device. The designer, therefore, has control over the type and thickness of material used in each layer of a heterostructure device, thus allowing the design of a specific response within the limits of the materials and the fabrication process. In order to understand the operation of heterojunction devices it is necessary to understand how these layers effect electron transport through the double barrier heterostructure.

The conduction band profile of Figure 4 shows the change in electron potential energy in the vertical (z) or epitaxial direction. This double barrier, quantum well structure gives rise to quasibound states in the quantum well whose energies can be found by solving the time independent Schroedinger equation for the structure. We first recall that for an infinitely deep quantum well, the bound energy levels would be given by Eq. 5. [Ref. 6]

$$E_n = \frac{(n\pi\hbar)^2}{2m^* L_w^2} \qquad (5)$$

$\hbar$ = 6.626 x 10^{-34} J - s / 2π

m^* = effective mass

L_w = quantum well width

For each of these energy levels, there are precisely a half-integer multiple of the electron wavelength that fit in the width of the quantum well. For the quantum well in the double barrier structure, however, the electrons are not truly bound as in the above example. Rather, they will be "quasi-bound", having a large lifetime in the quantum well, before the electron tunnels out. It is more appropriate, for

this statement, using the time independent Schroedinger equation, to solve for the probability that an electron will be transmitted through the structure. This transmission probability is given by Eq. 6. [Ref. 9]

$$T(E_z) = \left| \frac{A_E^R}{A_E^L} \right|^2 \qquad (6)$$

$$\frac{A_E^R}{A_E^L} = e^{-ik(2d+D)} \left[\left\{ \cosh(kd) - i \frac{2E_z - V}{2\sqrt{E_z(V-E_z)}} \sinh(kd) \right\}^2 e^{-ikD} + \frac{4V^2}{E_z(V-E_z)} \sinh^2(kd) e^{ikD} \right]^{-1}$$

$$k = \frac{\sqrt{2m^*(E_z - V)}}{\hbar}$$

A_E^R = fraction of electrons at collector

A_E^L = fraction of electrons at emitter

E_z = electron energy

V = height of the potential barrier

d = width of barrier

D = width of quantum well

Figure 5 shows the transmission probability vs. energy (E_z) under zero bias for a typical GaAs / AlGaAs heterostructure computed from Eq. 6. For most energies, there is a very small probability of electron transmission. Over a few narrowly defined ranges of energy, however, there are resonances in the transmission coefficient. At these resonant tunneling energies, the electron will essentially pass through the structure unimpeded. The resonance is determined by the action of constructive interference, where the wavelength of the electron

approximately matches the dimension of the quantum well. "Resonant tunneling is the electron analog of the Fabry-Perot resonator in optics." [Ref. 8]

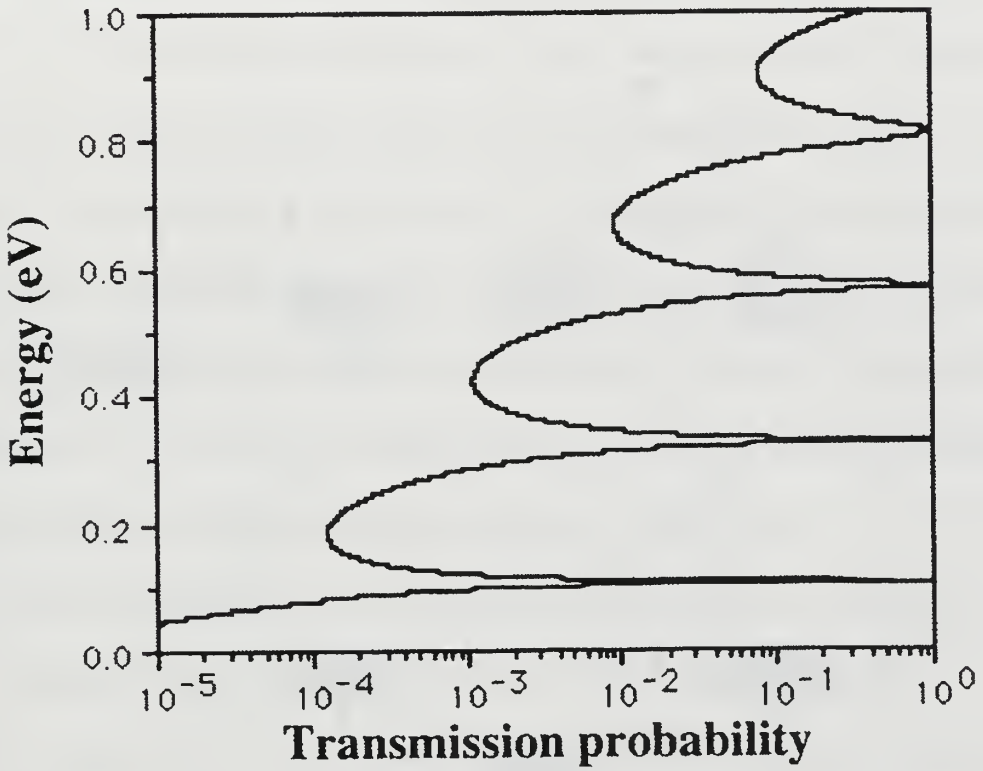

Figure 5 - Transmission probability versus energy for a GaAs / AlGaAs DBRTD under zero bias. From Ref. [9]

In Fig. 5, the transmission probability is shown as a function of electron energy. These resonances can effectively be used as an energy filter in a device application to control resonant transmission in the double barrier heterostructure. It is not practical to appreciably modulate the energy of individual electrons. Instead the device is biased (across the emitter and collector) to allow electrons (whose energies are a design criteria) to tunnel through the device. The action of the bias in essence modulates the energy of the transmission resonance relative

to the fixed (Fermi) energy of the electrons in the "leads" to the device. Figure 6 shows the conduction band profile of a typical GaAs / AlGaAs DBRTD under four bias states ((a)zero (b)threshold (c)resonance and (d)post resonance).

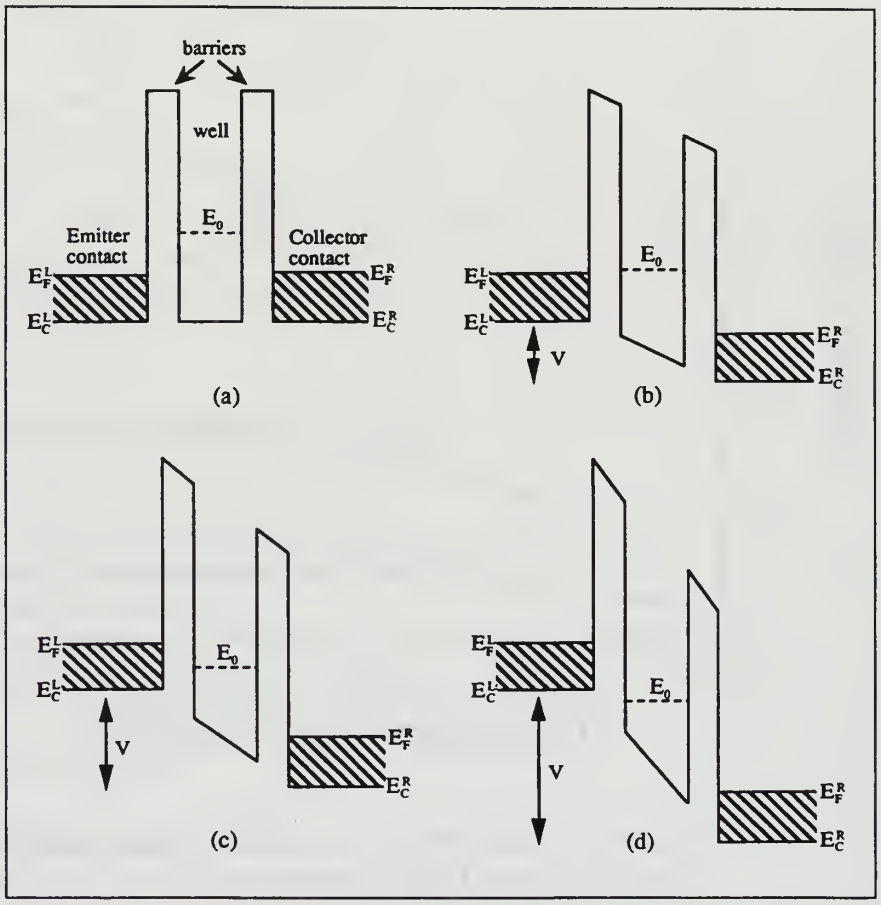

Figure 6 - DBRTD under four bias states. (a) no bias. (b)threshold bias. (c) resonance. (d) post resonance. From Ref. [9].

Here E_F^L (E_F^R) is the Fermi energy level or lowest unoccupied electron energy level in the emitter (collector). E_0 is the energy level at which resonant tunneling occurs, and E_C^L (E_C^R) is the conduction band minimum of the emitter (collector) material. Figure 6a shows the conduction band energy for an unbiased double barrier device. The energy of electrons in the emitter will typically be between

E_C^L and E_F^L, which we note are below the resonant tunneling energy, E_0. Hence no current flows in this configuration. In Figure 6b, a bias is applied such that the resonant tunneling energy level now lies just above E_F^L; hence, some electrons may tunnel through the barriers. In Figure 6c, a larger bias is applied such that the resonant tunneling energy level now lies between E_C^L and E_F^L. At this level of bias (resonance), a large fraction of the emitter electrons have their energy aligned with the tunneling resonance; there is now a substantial amount of tunneling and a maximum amount of current through the device. As the bias is increased further, the resonant tunneling level falls below the emitter band edge and the current flow drops precipitously (depicted in Figure 6d).

Just as the operation of the transistor is characterized by its response under an applied bias, the DBRTD is characterized in a similar way. It is, therefore, necessary to be able to calculate the current flow through a device in order to characterize its operation. The current flow (ie, the number of electrons transmitted through the structure) is determined by the number of electrons available to tunnel (Eq. 8) as well as the probability for transmission (Eq. 6). The total current [Ref. 9] is thus given as an integral over all electron energies,

$$J(V) = \int_0^\infty T(E_z)S(E_z)dE_z \qquad (7)$$

where T(E) is given by Eq. 6 and where S(E), the "supply" function, is given by Eq. 8. [Ref. 9]

$$S(E_z) = \frac{m^* e k_B T}{2\pi^2 \hbar^3} \ln\left[\frac{1+\exp\left(\frac{E_F^L - E_Z}{k_B T}\right)}{1+\exp\left(\frac{E_F^R - E_Z}{k_B T}\right)}\right] \qquad (8)$$

m^* = effective mass T = absolute temperature (K)

$e = 1.6 \times 10^{-19}$ coulombs $\hbar = 6.626 \times 10^{-34}$ J - sec

$k_B = 1.381 \times 10^{-23}$ J/K E_Z = electron energy

Note that the bias across the device is the difference in Fermi levels between emitter and collector. Figure 7 shows the current voltage response for a typical GaAs / AlGaAs DBRTD at 300 K. The graph has a close correspondence with Figure 6 where the current flow (level of resonant tunneling) can be discerned at each of the four bias states. In the unbiased as well as threshold biased states (Fig. 6a and Fig. 6b), there is effectively no current flow through the device. At resonance (Fig. 6c, 0.2V) there is a peak current flow. Finally, there is

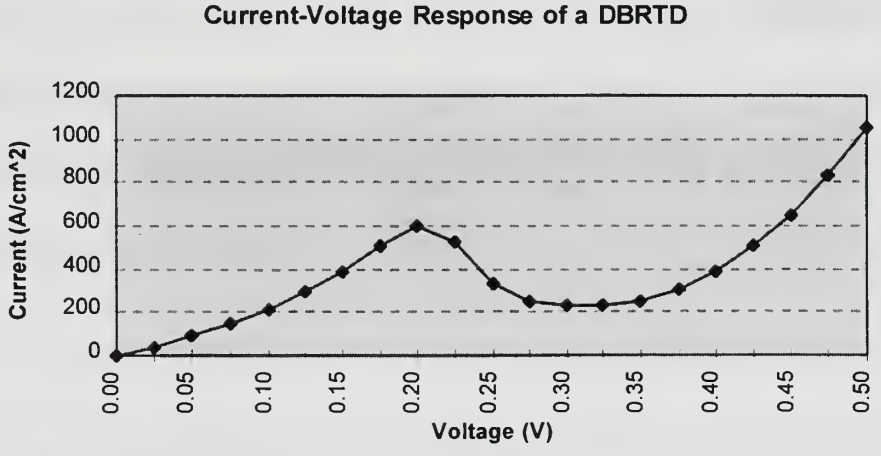

Figure 7 - Current versus Voltage for a GaAs / AlGaAs DBRTD.

dramatically diminished current flow in the post resonance bias state (Fig 6d, 0.3V).

As discussed earlier, the effective mass Schroedinger equation (Eq. 4) is an approximation used to determine the flow of electrons through the double barrier heterostructure. When solved it will give the probability that an electron will be at a specific location. One factor in the equation that is not yet known is the electrostatic potential. Determination of this single variable is no simple matter and is the discussion of the subsequent chapter.

IV. MODELING THE DOUBLE BARRIER RESONANT TUNNELING DIODE

A. FINITE TEMPERATURE THOMAS-FERMI THEORY

In order to determine the electrostatic potential in a heterostructure device, it is necessary to model the density of free electron charge carriers of each of the layers. One technique which has produced good results is the Thomas-Fermi theory. In this model the local electron density is taken to be that of a free electron gas in thermal equilibrium with the local value of the potential energy at temperature T(K) and under zero bias. In this model the electron density function is given by [Ref. 10]:

$$n(z) = N_c(z) F_{1/2}\left[\frac{\left(\mu - eV(z)\right)}{k_B T}\right] \qquad (9)$$

$$N_c(z) = 2\left[\frac{m^*(z) m_e k_B T}{2\pi\hbar^2}\right]^{3/2} \qquad (10)$$

$$F_\alpha(\eta) = \frac{1}{\Gamma(\alpha+1)} \int_0^\infty \frac{x^\alpha}{\left[1+\exp(x-\eta)\right]} dx \qquad (11)$$

N_c = density of states in the conduction band (Eq. 10)

F_α = Fermi-Dirac integral (Eq. 11)

m^* = effective mass $\qquad$ m_e = electron mass

μ = chemical potential $\qquad$ $k_B = 1.381 \times 10^{-31}$ J/K

V(z) = electrostatic potential $\qquad$ $\hbar = 6.626 \times 10^{-34}$ J - sec / 2π

As mentioned earlier the effective mass is a material dependent parameter and will be different for each layer of the double barrier heterostructure thus changing

the density of the free electron gas in each layer. Once the electron density function is given, the electrostatic potential (V) can be determined using a form of Poisson's equation given below as Eq. 12 [Ref. 10].

$$\frac{d}{dz}\left(\varepsilon(z)\frac{dV(z)}{dz}\right) = -e\left[N_D(z) - n(z)\right] \qquad (12)$$

$\varepsilon(z)$ = dielectric constant

e = 1.6 x 10^{-19} coulombs

N_D = number density of donors (~10^{18} /cm^3)

n(z) = density of the free electron gas (Eq. 10)

With the electrostatic potential function known, the transmission coefficient can be calculated using the time-independent Schroedinger equation, and, finally, the current flow through the device can be determined as discussed in the previous chapter.

B. POISSON-SCHROEDINGER THEORY

Another method for determining the potential in a heterostructure device is the self-consistent or Poisson-Schroedinger method. This method entails solving two distinct but also interconnected problems. As with the Thomas-Fermi theory, the electron density function must be determined in order to arrive at the potential function. In this model, the electron density is determined using Eq. 13 [Ref. 8].

$$n(z) = 2\sum_{k>0}|\psi_k(z)|^2 f_L(k) + 2\sum_{k<0}|\psi_k(z)|^2 f_R(k) \qquad (13)$$

$$f_L(k) = \left(\frac{k_B T}{4\pi^2 \hbar^2}\right) m^* \ln\left[1 + \exp\left(\frac{E_F^L - E(k)}{k_B T}\right)\right] \qquad (14)$$

$$f_R(k) = \left(\frac{k_B T}{4\pi^2 \hbar^2}\right) m^* \ln\left[1 + \exp\left(\frac{E_F^R - E(k)}{k_B T}\right)\right] \qquad (15)$$

n(z) = electron density (cm^{-3}) ψ_k = wave function

k = wave number $k_B = 1.381 \times 10^{-31}$ J/K

T = temperature (K) m^* = effective mass (kg)

$\hbar = 6.626 \times 10^{-34}$ J - sec / 2π E_F = Fermi energy level (eV)

E(k) = electron energy (eV)

Once the electron density is determined, using a given set of wave functions (ψ_K), the electrostatic potential can be determined from the Poisson equation using Eq. 17 [Ref. 8].

$$\frac{d}{dz}\left(\varepsilon(z)\frac{dV_{sc}(z)}{dz}\right) = -e\left[N_D(z) - n\left(V_{sc}(z)\right)\right] \qquad (16)$$

V_{SC} = self consistent electrostatic potential (V)

N_D = number density of donor atoms (cm^{-3})

n = number density of electrons (cm^{-3})

Eq. 13 and Eq. 16 are dependent upon each other and must be solved recursively using iterative techniques. In addition, the wave functions in Eq. 13 are dependent upon the effective-mass Schroedinger equation (Eq. 4) and must also be solved recursively. Thus, there are three inter-connected equations which must be solved simultaneously in order to obtain the electrostatic potential. Numerical techniques for gaining convergence to a solution will not be

discussed here but can be found in [Ref. 9]. As with the Thomas-Fermi theory, the electrostatic potential can now be used to determine the transmission coefficient using the Schroedinger equation and finally the current flow through the device.

The self-consistent method is computationally intensive and considerably more complex to employ than the Thomas-Fermi method. It is, however, the more accurate of the two and should be considered a baseline from which to evaluate the Thomas-Fermi method. Also, it is important to understand the limits of the Thomas-Fermi theory in modeling double barrier heterostructures.

C. COMPARISON OF THOMAS-FERMI AND POISSON-SCHROEDINGER THEORIES.

In order to compare the two solution methods, simulations were run using a nanoelectronic modeling program currently under development by Texas Instruments Incorporated and made available to the Naval Postgraduate School. Both simulations were run using the same structure at 300 K and an x-mole fraction in the AlGaAs of 0.4. Table 1 below shows a summary of the device structure. One simulation was run using the Thomas-Fermi method to model the potential profile in a 1-D double barrier heterojunction, while the second simulation was run using the Poisson-Schroedinger method.

Layer	Material	Thickness(nm)	doping (cm-3)
1	GaAs	3.00298	1x1018
2	GaAs	2.01143	2x1015
3	AlGaAs	0.45328	2x1015
4	GaAs	0.62326	2x1015
5	AlGaAs	0.45328	2x1015
6	GaAs	2.01143	2x1015
7	GaAs	3.00298	1x1018

Table 1 - Device structure used for simulations.

Figure 8 shows the electron density as a function of position in the device under four bias states. The peak bias state refers to the peak current or

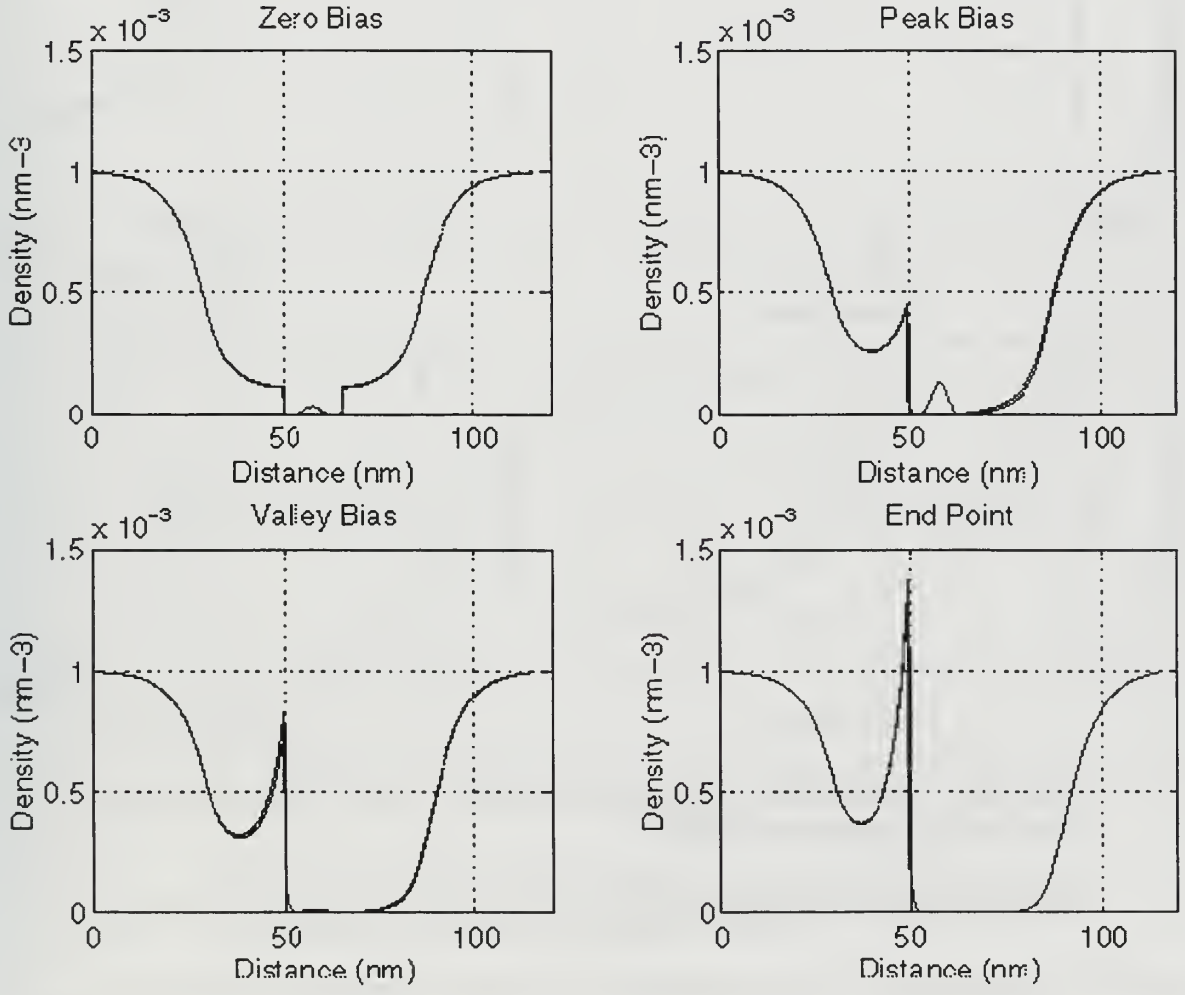

Figure 8 - Electron Density versus Location for the Thomas-Fermi and Poisson-Schroedinger Models.

resonance state. The valley bias state refers to the valley current or lowest current in the device at post resonance bias states. Each graph has a plot derived from the Thomas-Fermi model as well as from the Poisson-Schroedinger model. The two models have such similar results that it appears there is only one plot in all but a few places.

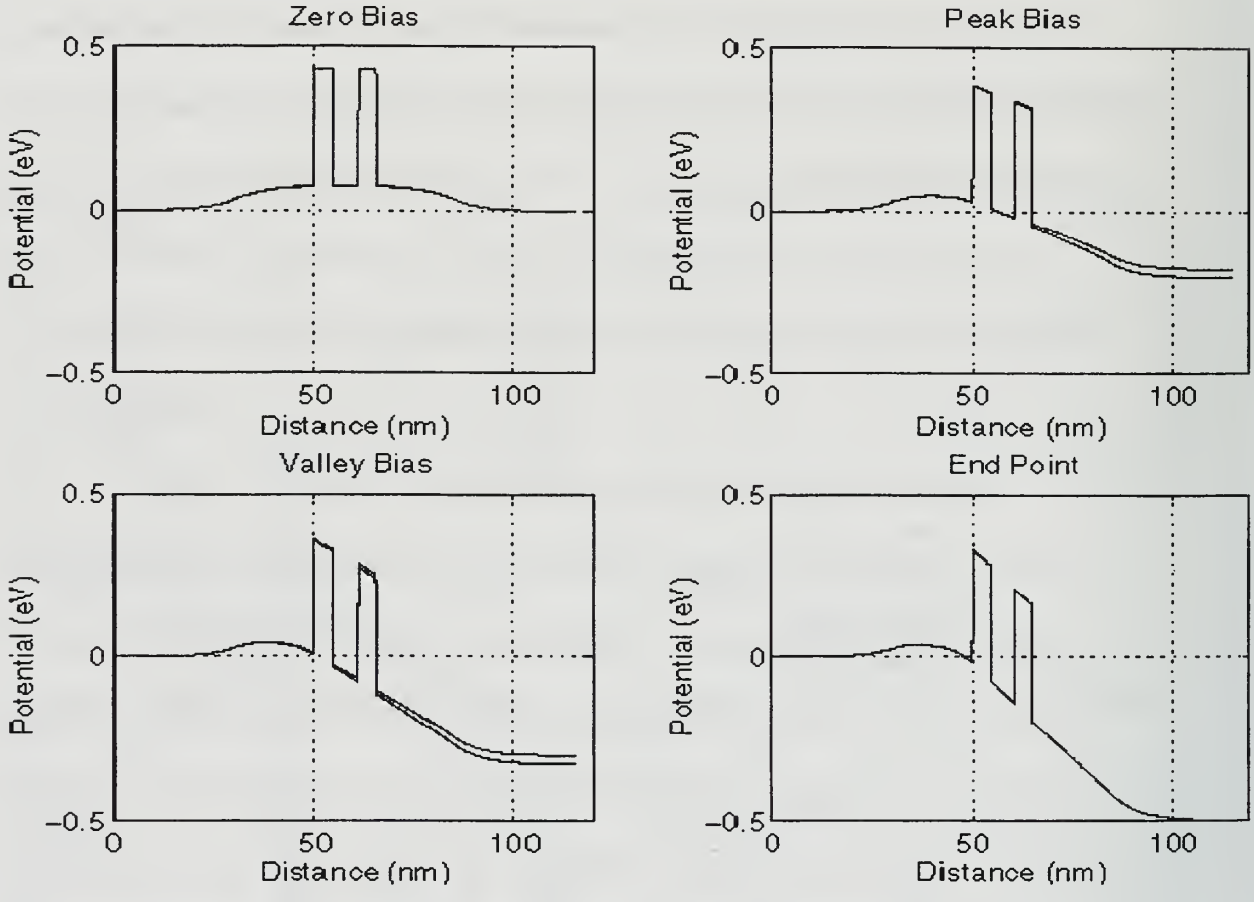

Figure 9 - Potential Energy versus Location for the Thomas-Fermi and Poisson-Schroedinger Models.

Figure 9 shows the total potential as a function of position in the device under four bias states. The bias states are similar to those seen in Figure 8 where the peak bias state refers to resonance and the valley bias refers to the

lowest current at post resonance states. At all four bias states the plots are very similar with a slight divergence in the collector at higher bias states.

Figure 10 is a comparison of the current-voltage characteristics of the two potential models computed using Eq. 7. The current-voltage characteristics of a device are, effectively, what the designer sets out to achieve when designing a device. The two plots are now discernible from each other but still very similar.

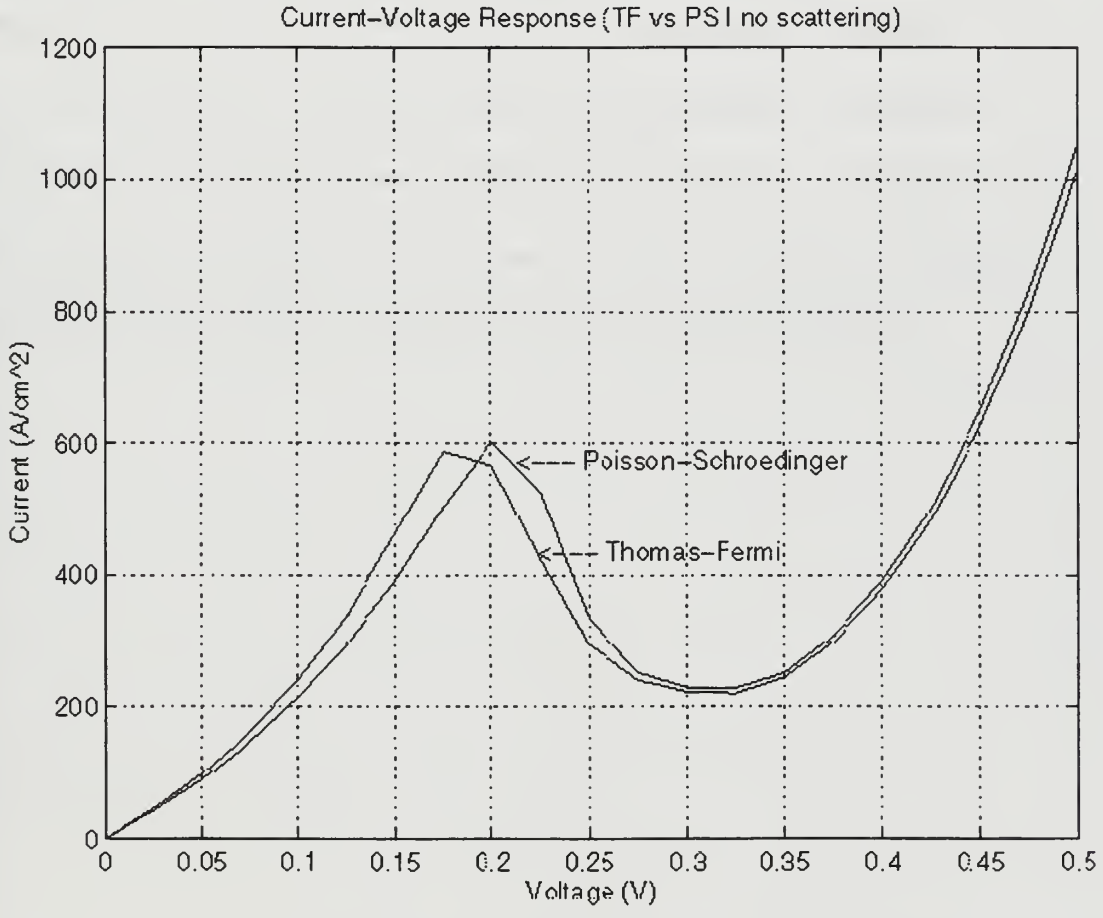

Figure 10 - Current versus Voltage Response for the Thomas-Fermi and Poisson-Schroedinger Models.

Under the conditions used for this comparison, the Thomas-Fermi theory provides a sufficiently robust theoretical basis upon which to determine the response of a device.

V. CONCLUSION

The continued downsizing of digital technology will require break throughs in device modeling, design and fabrication. Nanoelectronics and the use of the phenomenon of quantum mechanical resonant tunneling provides one possible alternative. Modeling the DBRTD is only the first step in developing this technology. Future efforts will need to validate nanoelectronics models by fabricating devices similar to those modeled (or vice versa). If successful, this effort can be expanded to model other device structures which can then be incorporated in the design of future generation microprocessors. Though still in its early stages, nanoelectronics and its use of quantum mechanical resonant tunneling may be the source of tomorrow's microprocessor technology.

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